RESUME

Name of the faculty Dr.Y.SYAMALA

Department: Electronics and Communication Engineering
College: Gudlavalleru Engineering College
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Address for Communication

F.No: 504, Brundhavan Apartments,

Opp.Dr.K.K.R's Gowtham School, Bypass Road,

Santhi Nagar, Gudivada-521301.

Academic Qualifications

S. No	Name of the Degree *(Starting from Ph.D to 10th Class)*	University	Percentage of Marks/Grade	Specialization	Year of Pass
1.	Ph.D	JNTUH, Hyderabad	Awarded	Low Power Digital VLSI	2014
2.	M.E	Anna University, Chennai	74%	Applied Electronics	2005
3.	B.E	Bharathiyar University, Coimbatore	66%	EIE	2001
4.	Intermediate	Board of Intermediate	66%	MPC	1997
5.	SSC	Z.P.H, School	80%	-	1995

Professional Experience: 14 Years

S. No	Designation	Institution Name	Working Period	
			From	To
1.	Associate Professor	Gudlavalleru Engineering College, Gudlavalleru	1.2.2011	Till date
2.	Senior Grade Assistant Professor	Gudlavalleru Engineering College, Gudlavalleru	1.7.2010	31.1.2011
3.	Assistant Professor	Gudlavalleru Engineering College, Gudlavalleru	1.7.2005	30.6.2010

Professional Body Membership: 02

S. No	Name of the Professional body	Membership Number
1.	IETE	M-216330
2.	ISTE	LM48528

Papers Published in Journals No. : 20

1. Patent Application Publication, "Magnetic Resonance Coupling Wireless Power Transfer Unit For Implantable Biomedical Devices", The Patent Office Journal No. 34/2020 Dated :21/08/2020, pp. 33088.
2. Venkata Latha. G , **Syamala.Y**, Anil Chowdary.T, Murali Krishna. G, " Reversible Vedic Multiplier", International Journal of Engineering and Advanced Technology (IJEAT), Vol.no.:8 Issue-6S2, PP: 852- 857, ISSN: 1876-1119, DOI: 10.35940/ijeat.F1211.0886S219, August, 2019 [SCOPUS].
3. E. Vijaya Babu, **Y. Syamala**, "Design and Analysis of Multiplexer Based 4-Bit Flash ADC", International Journal of Engineering and Advanced Technology (IJEAT), Vol.no.:8 Issue-6S2, PP: 797-802, ISSN: 1876-1119, DOI: 10.35940/ijeat.F1211.0886S219, August, 2019 [SCOPUS].
4. K Srilakshmi, A V N Tilak, K Srinivasa Rao and **Y Syamala**, "Energy Efficient 64-bit Asynchrobatic Adder", Book chapter, Springer Lecture notes in Electrical Engineering Book Series (LNEEE), Vol. 476, 2018, pp. 499-508.
5. S. Varshini, **Y.Syamala**, TVSSAN Murthy, "MIMO-UWB Radar System to Enhance the Energy Efficiency", International Journal of Innovations & Advancement in Computer Science (IJIACS), Vol. 6, Issue 9, pp. 2347 – 8616, 2017.
6. T.Suresh, C.Ramesh Reddy, **Y.Syamala**, A.V.N.Tilak, "Implementation of AFDX switch on ZYNQ FPGA", International Journal of Science and Research (IJSR), Vol. 5(7), pp: 2017-2024, 2016.

7. T. Durga prasad, K. Srilakshmi and **Y. Syamala**, "Design and implementation of energy efficient code converters", International Journal of computer science and information technology and Security, Vol. 6(4), pp. 33-36, 2016.
8. G.Venkatalatha, **Y.Syamala**, "Design and Implementation of Low Power Reversible ALU Using Parity Preserving Logic", IFRSA International Journal of Electronics Circuits ,and Systems Vol. 4 |issue 2, pp. 125-135, 2015.
9. K. Prudhvi Raj and **Y.Syamala**, "Transistor Level Implementation of Digital Reversible Circuits", International Journal of VLSI design and Communication Systems (VLSICS), Vol.5, No.6, pp. 43-61, 2014.
10. Mahesh.G, **Y.Syamala**, "Weather Data Logger Using ARM Processor", International Journal of Advanced Research in Computer Science and Software Engineering, Volume.3, Issue 9, pp: 1206- 1209, 2013.
11. Venkata Vinetha Kasturi and **Y Syamala**, "VLSI Architecture For DCT Based on Distributed Arithmetic ", International Journal of Engineering Research and Technology, Vol.2(5), 2013.
12. K. Srilakshmi, **Y.Syamala** and A. Suvir vikram, "Design and Implementation of CMOS VLSI Circuits using Dual Subthreshold Supply Voltages", International Journal of Engineering Research and Applications (IJERA), Vol. 3(5), 2013, pp: 1604-1608.
13. N. Somasehara varma, **Y. Syamala**, K. Srilakshmi, "Design of low power logic circuits using gate diffusion input(GDI) technique", International journal of VLSI design and communication systems (VLSICS), Vol. 4(5), 2013, pp. 89-95.
14. A. Suvir Vikram, K. Srilakshmi, **Y. Syamala**, "Static Power Optimization Using Dual Sub Threshold Supply Voltages In Digital CMOS VLSI Circuits", International journal of VLSI design and communication systems (VLSICS), Vol. 4(5), 2013, pp. 77-88.
15. **Y. Syamala**, K. Srilakshmi and N. Somasekhara Varma, "Design and Implementation of CMOS VLSI Digital Circuits Using Self-Adjustable Voltage Level Technique" International Journal of Engineering Research and Applications (IJERA), Vol. 3(5), 2013, pp. 1941-1946.
16. G.Hari Babu and **Y.Syamala**, "Testing of the Digital Circuits using Accumulator based BIST", International Journal of Engineering Science and Innovative Technology (IJESIT) Volume 2, Issue 6, pp. 294-299, November 2013.
17. **Y Syamala**, AVN Tilak, K Srilakshmi, "Testing of Reversible Combinational circuits", Springer Journal, pp. 46-53, 2012.
18. D. Sarvani, and **Y. Syamala**, " Realization of Reversible Full Adder and Reversible Full Subtractor using RPLA", International Journal of Engineering Research and Applications (IJERA) Advanced Signal Processing and Integrated Circuits, pp. 56-59, 2011.
19. Y.Ratna Babu and **Y.Syamala**, "Implementation and Testing of Multipliers using Reversible logic", IET Digital library, pp. 171-175, 2011.
20. **Y Syamala** and AVN Tilak, " Synthesis of Multiplexer and Demultiplexer circuits using Reversible Logic", International Journal on Recent Trends in Engineering and Technology, Vol. 4 (3), pp. 34-38, 2010.

Papers Published in Conferences No. : 22

1. K. Srilakshmi, A V N Tilak, K. Srinivasa Rao and Y. Syamala, "Secured MPFAL Logic for IoT Applications", Proc. of 2nd International conference on Device,

Circuit and System (2020 IEEE VLSI DCS), July 18-19, 2020.

2. D.Bindusree, M.Srividya,Dr.Y.Syamala, " Remote Laboratory for Implementation of Various Applications Using Linear and Digital IC's", 16th International Conference on Remote Engineering and Virtual Instrumentation (REV2019), 02/03–06 February 2019.
3. K. Srilakshmi, A. V. N Tilak and Y. Syamala, " Development of Low-Power VLSI Circuits for Biomedical Applications" Proc. of CITAES 2018.
4. E. Vijaya Babu, Y. Syamala, K. Srilakshmi and K. Siva Anjaneyulu, "Design and analysis of multiplexer based flash ADC", Proc. of CITAES 2018.
5. G.Venkata Latha,, Y. Syamala, T.Anil Chowdary, and G.Murali Krishna,"Reversible Vedic Multiplier", Proc. of CITAES 2018.
6. **Syamala.Y**, Tilak A.V.N, Srilakshmi.K and Anil Chowdary. T, "Low Power Testable Reversible Combinational Circuits", Proc. of Second IEEE International Conference on Intelligent Computing and Control Systems (ICICCS) during 14th-15th June 2018.
7. G.Venkata Latha and **Y.Syamala**, "Design and Implementation of Reversible Vedic Multiplier", Proc.of 9th IIAR International Conference-LTNEESAMALPMS- during 25th -26th March 2018.
8. K. Srilakshmi, A. V. N Tilak, K. Srinivasa Rao and **Y. Syamala**, "Energy Efficient 64-Bit Asynchrobatic Adder" , Proc. of International Conference on Nano-electronics, Circuits and Communication Systems (NCCS-2016).
9. B N V Amar Surendra Babu, **Y Syamala** and K Srilakshmi, "Design and Implementation of Power Optimized 64 Bit Floating Point ALU Employing Block Enabling Technique", 4th International Conference on Innovations in Electronics & Communication Engineering, Hyderabad during 21-22nd August 2015.
10. **Y.Syamala**, A.V.N.Tilak and K.Srilakshmi, "Testing of Reversible Combinational Circuits", 3rd International Conference on Advanced in Communication Networks & Computing Feb 24-25, 2012, Chennai.
11. M.V. Narayana, G. Ashok, **Y. Syamala** and K. Srilakshmi, "Low Power CMOS Digital Design Using Adiabatic Logic", ICVSP-2012, 4-5 May 2012, Bangalore.
12. B. Kavya sree, **Y.Syamala** and K.Srilakshmi, "Transistor Realization of Reversible parallel adder/subtractor", National Conference on VLSI, Signal Processing and Communications, 5-6 Feb 2012,Vadlamudi,Guntur.
13. **Y.Syamala** and Y.Ratnababu, "Implementation and Testing of Multipliers using Reversible logic", International conference on ARTCOM, Sep 13-14, 2011, Bangalore.
14. **Y.Syamala** and B. Kondalu, "Power Optimization technique for digital circuits using scan based BIST", National conference on signal processing and Embedded systems applications, July 8-10, 2011, Chennai.
15. **Y.Syamala** and A.V.N. Tilak, "Reverisble Arithmetic Logic Unit", International Conference on Networking and computer science (ICNCS-2011), April 8-10,2011, Singar Int.Hotel, Kanyakumari.
16. **Y.Syamala** and A.V.N. Tilak, "A Low power BIST TPG with gated clock scheme", International Conference on advances in Information , Communications

Technology and VLSI Design (ICAICV-2010), Aug 6-7 , 2010, PSG College of Technology, Coimbatore.

17. Ch.Sowjanya and **Y.Syamala**, "Design and ASIC Implementation of Root Raised Cosine Filter", International Conference on Emerging Trends in Signal Processing & VLSI Design SPVL, June 11-13, 2010, Gurunanak Engg College Ibrahimpatnam, Hyderabad.
18. **Y.Syamala** and A.V.N. Tilak, "An effective BIST scheme for parallel adders",International Conference on Emerging Trends in Signal Processing & VLSI Design, June 11-13, 2010, Gurunanak Engg College Ibrahimpatnam, Hyderabad.
19. S. Ratna Satya Kishore, **Y.Syamala** and M.Kamaraju, "FPGA Implementation of Digital Time slot Interchanger (DTSI)", NCASP-09, Nov.20-21, Hyderabad.
20. M.Kamaraju, BVSL Bharathi and **Y Syamala**, "Remote Observation and Control System for Military Surveillance", International Conference, Feb.26-27, 2009, SCT College of Engineering, Trivandrum.
21. **Y.Syamala**, Latha, "High performance FIR filter Design based on sharing multiplier", National Conference on Emerging technologies in Electronics & Communication, BIHER, 2005, Chennai.
22. **Y.Syamala**, Latha, "High performance FIR filter Design based on sharing multiplier", National Conference on CITEL, 2005.

Workshops Organized No. : 04

1. One week live webinar and workshop on "Performing And Designing Experiments With Virtual platform, Hands on session, organised by Gudlavalleru engineering college in association with IITR during 24th - 28th August 2020.
2. Three day World space week "Student competitions", organized by ISRO-GEC, Gudlavalleru Engineering College, Gudlavalleru during 6th – 8th October 2018.
3. Two day workshop on "Embedded System Development", organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 30th - 31st December 2013.
4. One week faculty refresher course on "Electronic Devices and Circuits" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 9th – 13th June 2014.

Workshops /Conferences /Seminars Attended No. : 20

1. Two day workshop on Virtual and Remote labs, organized by 16th International Conference on Remote Engineering and Virtual Instrumentation (REV2019), 03–06 February 2019.
2. Two day workshop on Virtual and Remote labs, organized by APSSDC-IUCEE, during 27th-28th September 2018.
3. Two day workshop on Analog VLSI Design, Organized by C-DAC, Bangalore during 22nd -23rd January 2016.
4. One day workshop on ultra Low Power Communication using CC430 Microcontroller::

Hands on Experience, Organized by Signal processing and Communications research group, ECE at GEC, Gudlavalleru on 7th February 2015.

5. One day seminar on Research in signal and image processing on FPGA's and Embedded Platforms, Organized by IE Vijayawada Local centre, Vijayawada on 22nd November 2014.
6. One day workshop on Speech Processing and Current Challenges and Hands-on Experience, Organized by Signal processing and Communications research group, ECE at GEC, Gudlavalleru on 23rd August 2014.
7. Two Week ISTE Workshop on Signals &Systems Conducted by IIT Kharagpur, under the National MHRD program at GEC, Gudlavalleru from 2nd to 12th January 2014.
8. Two day workshop on Issues in Integrated Circuits, Organized by Department of ECE at GEC, Gudlavalleru on 13th-14th December 2013.
9. One week refresher course on Electronic Devices and circuits at GEC, Gudlavalleru during 23rd- 28th September 2013.
10. Two Week ISTE Workshop on Analog Electronics Conducted by IIT Kharagpur, under the National MHRD program at GEC, Gudlavalleru from 4th to 14th June 2013.
11. Two day National workshop on Advanced VLSI Technology Organized by University College of Engineering, JNTUK, Kakinada on 26th &27th April 2013.
12. Two day ISTE work shop on Aakash for Education conducted by IIT Bombay in association with department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 10th -11th November 2012.
13. 25th International Conference on VLSI Design & 11th International Conference on Embedded Systems, Novatel complex, HICC, Hyderabad, 9th -10th January 2012.
14. One day Workshop on Analog, Digital and Mixed Signal VLSI Design Organized by ECE, GEC, Gudlavalleru on 15th October 2011.
15. Two day Workshop on VLSI design software TANNER TOOLS, JNTU, Kakinada, 27th-28th September, 2008.
16. Functional approaches to VLSI Technology and Design, GNITS-Hyderabad during 12th - 14th February 2007.
17. Workshop on VLSI Design Organized by Department of ECE at GEC, Gudlavalleru during 9th & 10th February 2007.
18. Two days FDP on VLSI and Embedded system design at GEC, Gudlavalleru during 7th &8th July 2012.
19. One day national workshop on Wireless Communication and Networks organized by department of ECE, Kumaraguru College of Technology, Coimbatore on 9th October 2004.
20. Two day workshop on Modern Tools in Electrical Engineering organized by department of EEE, Kumaraguru College of Technology, Coimbatore during 27th & 28th of February 2004.

Online Workshops /Conferences /Seminars Attended No. :03

1.Workshop on "Reference Management tools and Online Citation Database" with grade A , organised by Indian Academic Researches Association, during 21st to 23rd May 2020.

2. Attended workshop on "**VLSI circuits Analog and Digital Design perspectives**", organised by Department of Electronics and Communication Engineering JNTUA college of Anantapuramu in association with AMS Semiconductors and HCL Technologies during 16th - 17th May 2020.

3. Attended two day online workshop on " **Modern Methods for Teaching-Learning Practices**", organised by Krishna University on 12th - 13th May 2020.

Webinars attended No.: 09

1. Webinar on Low Power VLSI Circuits and Energy Harvesting for IoT Applications, organised by department of electronics and Computer engineering, Sreenedhi institute of science and technology, Hyderabad during 15th August 2020.
2. A National Level Webinar on Intellectual Property Rights & Patents - A View organized by IQAC, Gudlavalleru Engineering College, Gudlavalleru held during 10 - 12 August 2020.
3. Attended a webinar on "**Impact of COVID in Engineering Education and Way Forward**", organised by ISTE chapter, Gudlavalleru Engineering College on 9th June 2020.
4. A webinar on "**Labview –Programming for Real-Time Applications**", Organised by Department of Electronics &Communication Engineering, Lakireddy Bali Reddy College of Engineering on 1st July 2020.
5. A webinar on "**Radio frequency Measurements for cellular and wireless Communication Systems**", organised by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College on 25th May 2020.
6. Attended Webinar on "**Winning the Competitive World**", Organised by Department of Electronics and Communication Engineering, SNS College of Technology on 4th May 2020.
7. AWebinar on "**Enhancing Research Effectiveness using Scopus, Science direct and Mendeley**", organised by Kurukshetra University on 1st May 2020.
8. Attended Webinar on " **Research Outcomes: Technical Paper Writing, Research Proposal, Patent Filing**", organised by Datateach on 22nd April 2020.
9. A Webinar on " **Analog IC Design Using Mentor EDA Tools**", organised by CoreEL Technologies and Xilinx on 10th April 2020.

Certifications/Training Programs Attended No. : 08

1. One week FDP on "Data Acquisition and RT using LabVIEW" organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru in association with National Instruments, Bangalore, during 25th to 30th November 2019.
2. Three day training program on Advanced "Development Tools Based IoT" organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 11th to 13th November 2019.
3. One week faculty development program on "Communications and signal processing" organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 29th October to 3rd November 2018.
4. Two day training program on "Mentor Graphics Tools" organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 31st August and 1st September 2017.
5. Two day training program on "Analog and Digital CMOS IC Design flow using Mentor graphics EDA Tools" Department of ECE, Shri Vishnu Engineering College for Women, Bhimavaram from 5th-6th October, 2015.
6. One week short term course on Advances in VLSI signal processing at IIT, Kharagpur during 3rd-7th December 2013.
7. Training on MATLAB, Simulink &Related Tool Boxes for Engineering Eductaion, Organized by GEC, Gudlavalleru on 3rd & 4th April 2013.
8. Five day Training Program on Mentor Graphics (Front end &back end) and Xilinx Tools, organized by IETE Vijayawada centre & ISF-GEC, &Corel Technologies, Bangalore, at GEC, Gudlavalleru from 13th to 17th September 2010.

Online Certifications/Training Programs Attended No. : 13

1. AICTE sponsored online Short Term Training program on Block chain Architecture and use cases Phase I organised by department of electronics and communication engineering, Gudlavalleru engineering college during 10th -15th August 2020.
2. One week refresher course on Embedded system design organised by department of electronics and communication engineering, Gudlavalleru engineering college during 27th July-1st August 2020.
3. Completed APSSDC online FDP on Internet of Things during 13th-25th July 2020.
4. Three day Hands on Online Faculty Development Program on "**Online Teaching Tools**", organised by Department of master of computer Application, Jain University during 8th - 10th July 2020.

5. Participated in Three day Hands on Online Faculty Development Program on "**Scientific Communication For Research Paper and proposal Writing**", organised by Department of master of computer Application, Jain University during 1st -3rd July 2020.
6. Five day online Faculty Development Programme on "**Opportunities and Challenges in Next - Generation Semiconductor Devices**", organised by Department of Electronics and Communication Engineering, Anil Neerukonda Institute of Technology and Sciences, during 16th - 20th June 2020.
7. Attended one week online Faculty Development programme on "**Electronics and Communication Engineeringnt Trends and Research Areas in Applied VLSI and Advanced Communicatons**", organised by Department of Electronics and Communication Engineering,Vasireddy Venkatadri Institute of Technology during 8th-12th June 2020.
8. One week international online Knowledge development program on "**Challenges And Advancements In The Design Of IoT, VLSI And Embedded Systems: A Researcher View**", organised by Department of Electronics and Communication Engineering of Gudlavalleru Engineering College during 8th- 13th June 2020.
9. Successfully completed Online Faculty Development Program on "**Embedded Systems**", organised by APSSDC during 25th May - 6th June 2020.
10. Online faculty Development Program on "**Artificial Intelligence and its Applications**", organised by Department of Computer Science and Engineering in collaboration with 360DigiTMG , Ramachandra College of Engineering During 25th - 30th May 2020.
11. Five day online Faculty Development Program on "**Trends in Communication**", organised by the Department of Electronics and Communication Engineering in association with Averzs Technologies Sir C R Reddy College of Engineering during 26th - 30th May 2020.
12. A three day Faculty Development Program on "**VLSI Digital Circuits and Testing Techniques**", organised by Department of Electronics and Communication Engineering ,Miracle Educational Society Group of Institutions during 21st - 23rd May 2020.
13. Successfully completed Online Certification Skill Development Program on "**Design Implementation and Verification in VLSI**", organised by Sandeepani School of Embedded System Design, during 27th April - 1st May 2020.

Guest Lectures Delivered No. : 04

Delivered lectures in ECE department staff seminars

- Adiabatic logic
- CPLD and FPGA
- Low voltage CMOS
- Spintronics

Subjects Handled

Under Graduation

- VLSI Design
- Digital IC Applications
- Linear IC Applications
- Switching Theory Logic Design
- Digital Circuit Design
- Linear and Digital IC Applications
- Low Power VLSI Design

Post Graduation

- VLSI Technology &Design
- Low power VLSI Design
- Analog & Digital IC Design
- CPLD & FPGA Architectures
- Principles of Digital Design using FPGA
- CMOS Analog and Digital Design

Labs Handled

Under Graduation

- ECAD
- Linear IC Applications
- IC &PDC
- Electronic Devices & Circuits
- VLSI and ES
- VLSI Design

Post Graduation

- HDL Programming

Other Responsibilities

College Level

1. Coordinator for labs and library development
2. Coordinator for Grievances and Redressal
3. Joint Secretary – Faculty Club
4. Academic Development
5. Coordinator for Various Events in GECFEST/Annual Day
6. Co-Convener for GECFEST'19

Department Level

1. Faculty Advisor - ECSAT
2. Class Teacher –III B.Tech
3. IC lab in-charge
4. Academic Coordinator
5. Internal R&D Coordinator
6. Department NAAC Coordinator

7. Department NBA Criteria 4 and 9 Coordinator
8. Associate Mentor under academic strengthening and advancement cell
9. BoS Member in ECE
10. R&D lab incharge

Projects Guided -Under Graduation:18; Post Graduation:15

Guiding Ph. D Students

University	Year of Registration	Area	Status
JNTUK	2018	VLSI	REGISTERED
JNTUK	2016	VLSI	REGISTERED

Books Published No. : 02

1. Co-author of book entitled "Electronics and Communication Engineering laboratory Manual" with ISBN – 978-1-4276-5536-3.
2. Co-author of book entitled "Electronics and Communication Engineering Instructional Material" with ISBN – 978-1-4276-5539-4.

R&D and Consultancy

S. No	Project Title	Source of Funding	Duration	Role	Status
1	Design and Development of Wearable Medical Sensors based Health	Internal R&D	2017-18	Co-Principal Investigator	Applied
	Monitoring system				
2	Design of low power Adder/Subtractor circuits using Reversible Logic	Internal R&D	2013-14	Principal Investigator	Completed

Curriculum Design and Development

1. VLSI Design
2. Digital IC Applications
3. Linear IC Applications

Extra Curricular Activities

1. Acted as BoS member for department of ECE, Gudlavalleru Engineering College, Gudlavalleru on 2nd August 2014 and 25th May 2015.
2. Acted as Judge for "Technical Paper Contest – GECFEST 2014" conducted by Gudlavalleru Engineering College.

Declaration

I hereby declare that all the above-furnished information is correct to the best of my knowledge.

Date: 26.08.2020

Signature

Place: Gudlavalleru (Y.Syamala)